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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,206	12/30/2003	Kee-Hoon Choi	11038-138-999	1857

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MORGAN, LEWIS & BOCKIUS, LLP.
2 PALO ALTO SQUARE
3000 EL CAMINO REAL
PALO ALTO, CA 94306

EXAMINER	
CHANDRAN, BIJU INDIRA	
ART UNIT	**PAPER NUMBER**
2835	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/749,206	CHOI, KEE-HOON
	Examiner	Art Unit
	Biju Chandran	2835

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. (US 6,239,973 B1), in view of Magnuson et al. (PGPub: US 2003/0209799), and further in view of Getkin et al. (PGPub US 2003/0171006).

   - Regarding claim 1, Taylor et al. disclose a cooling structure for an electronic element, wherein the structure comprises: an extended portion formed on an inner conductor (32) and contacting an upper surface of a heat-producing electronic element (column 2, lines 20-22, lines 45-50), wherein the inner conductor and the heat-producing electronic element (column 2, line 21) are mounted on an inner circuit substrate (12); a conductor case (made up of 20, 24 and 22) surrounding the inner conductor, the extended portion, the heat-producing electronic element, and the inner circuit substrate, the conductor case having an upper side and a lower side (marked in the figure); and a plurality of conductor case holes (marked) through the lower side of the conductor case; an external circuit substrate (16) with an upper side (14) and a lower side, wherein the upper side of the

external circuit substrate further comprises a heat sink (30) contacting the lower side of the conductor case; and a plurality of external circuit substrate holes (42) through external circuit substrate to correspondingly communicate with said conductor case holes of said conductor case. While Taylor et al. does not explicitly disclose that the inner conductor contacts the heat-producing electronic element, it would have been obvious to a person of ordinary skill in the art that the microprocessor (column 2, line 20) will be in contact with the inner conductor (32) in order to allow the heat from the processor to be removed from the system (column 1, lines 19-23). Taylor et al. do not disclose a plurality of through holes formed on the inner circuit substrate underneath the heat-producing electronic element, or a radiating plate mounted on the upper side of the conductor. Magnuson et al. disclose a semiconductor substrate with a plurality of through holes (Magnuson et al., paragraph 0012, figure 3, figure 4). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the inner substrate disclosed by Taylor et al. by incorporating a plurality of through holes as taught by Magnuson et al., under the heat producing electronic element to provide conductive interconnection between the front side and the back side of the substrate (Magnuson et al., paragraph 0003).

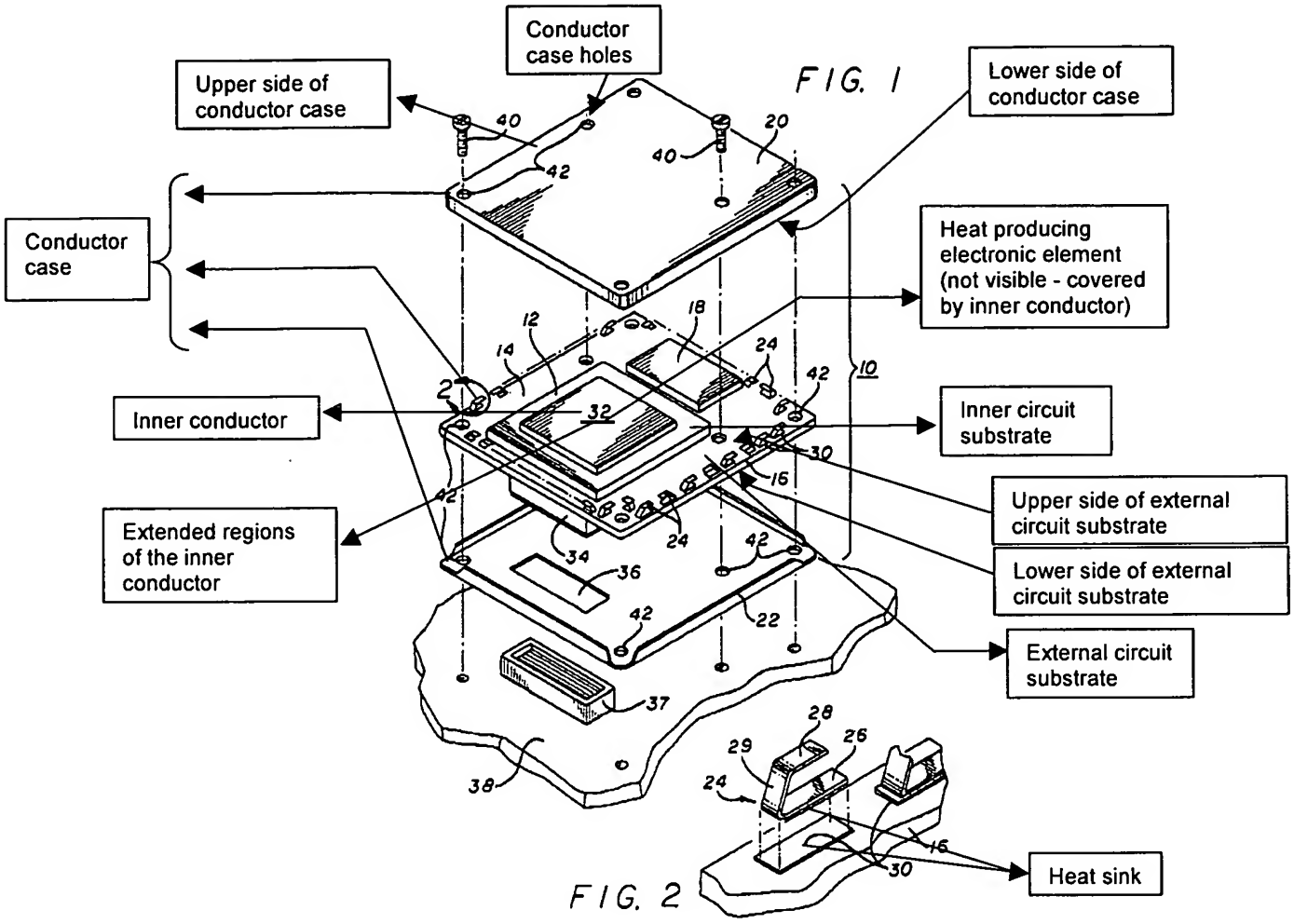

FIG. 1

FIG. 2

Getkin et al. disclose a heat producing electronic element attached to a substrate having a conductor with an extended portion contacting the heat-producing electronic element; and a radiating plate mounted on the upper side of the conductor (Getkin et al., figure 1B). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the radiating plate taught by Getkin et al. in the electronic element cooling structure taught by Taylor et al. to more effectively dissipate the heat generated by the

electronic element and improve its reliability and performance (Getkin et al., paragraph 0025, paragraph 0004).

- With respect to Claim 3, Taylor et al further discloses that the heat sink is a flat surface made of metal formed on the said external circuit substrate. With regard to the process of forming the heat sink, even though the claims are limited by and defined by the recited process, the determination of patentability of the product is based on the product itself, and does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made from a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

- With respect to Claim 4, while it is unclear what metal is used for the heat sink in Taylor et al., it would have been obvious to one of ordinary skill in the art to use any known metal conventionally used for heat dissipation based upon routine experimentation. It has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re. Leshin*, 125 USPQ 416.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. in view of Magnuson et al. and Getkin et al. as applied to claim 1, and further in view of Macris (US 6,686,532 B1). Taylor et al. does not explicitly state that the electronic element is a power amplifying module of a code division multiple access modem. Macris discloses a cooling structure for power amplifying module of a modem (Macris, column 1, lines 20-22). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the power amplifying module taught by Macris in the electronic element cooling structure taught by Taylor et al. to utilize its cooling capability.

Response to Arguments

Applicant's arguments filed on 12/22/2005 have been fully considered but they are not persuasive. Described below are the reasons why.

The applicant argues that:

> Taylor et al. disclose an integrated circuit package (12), which is itself a heat-producing electronic element (column 1, lines 19-20, cited by the Examiner as teaching a heat-producing electronic element, disclose integrated circuits, and column 1, lines 16-17 disclose integrated circuits assembled into integrated circuit packages such as integrated circuit package 12), not an inner circuit substrate as alleged by the Examiner. Taylor et al. do not disclose a heat-producing electronic element mounted on an inner circuit substrate; for at least this reason, claim 1 and its dependents claims 3-5 are patentable over Taylor et al.

Taylor discloses in column 1 line 19 that "Each integrated circuit generates heat which must be removed from the package", and further discloses in column 2 line 20-21 that that the "integrated circuit package 12" contains a high speed integrated circuit such as a microprocessor. These statements indicate that the microprocessor which is mounted on the package 12 in Taylor et al. is a heat producing electronic element. Also, it is well known in the art that microprocessor is a "heat producing electronic element".

The applicant does not disclose that the "inner circuit substrate" holds any special meaning, or does any special function other that supporting the heat producing electronic element and supporting the heat transfer functions of the conductors. The term "inner circuit substrate" also does not hold a special meaning in the relevant art, other than that of a conventional electronic packaging substrate (Pradeep Lal, Packaging Reliability, Chip-Scale Semiconductor, Package Architecture – An Overview, Wiley Encyclopedia of Electrical and Electronics Engineering, John Wiley and Sons, 1999, pages 516-518). The element marked '12' is part of the integrated circuit package in Taylor et al. that serves the same function as the "inner circuit substrate in the applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Biju Chandran whose telephone number is (571) 272-5953. The examiner can normally be reached on 8AM - 5PM. Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached on (571) 272-2092. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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LYNN FEILD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800